

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S29	6	"6524935"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/22 13:06
S30	862	("SiGe" 'sige' silicon near3 geranium) with (strained relaxed)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/22 14:23
S31	632	S30 and (implant\$3 nitridation nitrify nitrification inject\$3 silicide silicidation)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 09:02
S32	632	S30 and (implant\$3 nitridation nitrify nitrification inject\$3 silicide silicidation oxynitridation)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 09:03
S33	175	S32 and ("SiGe" 'sige' silicon near3 geranium) with (crystalline ((mono single) near3 (crystal crystalline)))	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 09:07
S34	166	S33 and ("SiGe" 'sige' silicon near3 geranium) with ('soi' insulat\$3 substrate)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 09:08
S35	166	S34 and (nitride silicon oxynitride nitrogen germanium metal metali\$4 heat\$3 anneal\$3 oxide)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 10:16
S37	1	S35 and vacan\$3	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 09:12
S38	95	S35 and \$4nitrid\$7	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 18:08
S39	10	"6455398"	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/21 18:08

S40	1	10/765999	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/22 13:07
S41	1076	("SiGe" "GeSi" 'sige' 'gesi' silicon near3 geranium) with (strained strain relaxed relaxation)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/22 14:31
S42	1076	S41 and ("SiGe" "GeSi" 'sige' 'gesi' silicon near3 geranium strained strain relaxed relaxation)	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/22 14:32
S43	37	S42 and strain\$3 near3 inducing	US-PGPU B; USPAT; EPO; JPO	OR	ON	2005/04/22 14:32

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L1: (58) "6059895" [S] [X]

T2: (0) 10/714130 [S] [X]

Document I Issue Date Page Title Current O Current X Retrieval Inventor S C P [S] [X]

1 US 2005007 2005033 6 METHOD OF FORMIN 438/406 438/197; Rim, Kern [S] [X]

2 US 2005000 2005011 10 Process for producing se 438/407 438/455; Cheng, Zhi-Yuan et al. [S] [X]

3 US 2004017 2004090 12 Semiconductor substrate 257/19 257/E21.1 Cheng, Zhi-Yuan et al. [S] [X]

4 US 2004016 2004090 10 Multiple gate MOSFET s 257/411 Rim, Kern [S] [X]

5 US 2004007 2004042 18 CMOS integrated circuit 257/347 257/E21.4 Bae, Geum-Jong et al. [S] [X]

6 US 2003016 2003091 15 Process for producing se 257/19 257/12; Cheng, Zhi-Yuan et al. [S] [X]

7 US 2003015 2003082 15 Process for producing se 257/12 257/78; Cheng, Zhi-Yuan et al. [S] [X]

8 US 2003007 2003042 6 Method of forming strain 438/478 257/E21.1 Shih, Wong-Cheng [S] [X]

9 US 2002014 2002100 7 Strained silicon on insula 257/347 257/E21.5 Rim, Kern [S] [X]

10 US 2002007 2002061 15 Process for producing se 438/10 257/616; Cheng, Zhi-Yuan et al. [S] [X]

11 US 6882025 2005041 22 Strained-channel transit 257/510 257/374; Yeo; Yee-Chia et al. [S] [X]

12 US 6881650 2005041 11 Method for forming SOI s 438/481 438/311; Lee; Jung-Il et al. [S] [X]

13 US 6881632 2005041 25 Method of fabricating C 438/285 438/199; Fitzgerald; Eugene [S] [X]

14 US 6878610 2005041 9 Relaxed silicon germaniu 438/478 Lin; Chun Chich et al. [S] [X]

15 US 6876010 2005040 14 Controlling threading disl 257/191 257/190; Fitzgerald; Eugene [S] [X]

16 US 6867433 2005031 19 Semiconductor-on-insula 257/67 257/350; Yeo; Yee-Chia et al. [S] [X]

17 US 6864115 2005030 13 Low threading dislocatio 438/37 438/87 Fitzgerald; Eugene [S] [X]

18 US 6858502 2005022 23 High speed composite p-c 438/285 438/172 Chu; Jack Oon et al. [S] [X]

19 US 6855992 2005021 44 Structure and method for 257/378 257/16; Eiprick; Rudy M. et al. [S] [X]

[S] [X] [S] [X]

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U	1	Document I	Issue Dat	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	A	B	C	D
20		US 6849883	2005020	15	Strained SOI MOSFET d	257/192	257/190;		Okihara; Masao	P						
21		US 6831292	2004121	13	Semiconductor structures	257/19	257/18		Currie; Matthew et	P						
22		US 6830976	2004121	25	Relaxed silicon germaniu	438/287	438/300;		Fitzgerald; Eugene	P						
23		US 6815738	2004110	10	Multiple gate MOSFET s	257/256	257/213;		Rim; Kern	P						
24		US 6815279	2004110	35	Manufacturing method of	438/199	257/369		Yagishita; Atsushi e	P						
25		US 6787852	2004090	7	Semiconductor-on-insula	257/347	257/348;		Yu; Bin et al.	P						
26		US 6787793	2004090	10	Strained Si device with fir	257/19	257/15;		Yoshida; Akira	P						
27		US 6770134	2004080	27	Method for fabricating w	117/89	117/103;		Maydan; Dan et al.	P						
28		US 6765227	2004072	8	Semiconductor-on-insula	257/19	257/192;		Yu; Bin et al.	P						
29		US 6750130	2004061	13	Heterointegration of mate	438/607	257/E21.5		Fitzgerald; Eugene	P						
30		US 6737670	2004051	18	Semiconductor substrate	257/19	257/E21.1		Cheng; Zhi-Yuan et	P						
31		US 6730551	2004050	11	Formation of planar strai	438/191	257/E21.6		Lee; Minjoo L. et al	P						
32		US 6724008	2004042	28	Relaxed silicon germaniu	257/19	257/190;		Fitzgerald; Eugene	P						
33		US 6723661	2004042	28	Relaxed silicon germaniu	438/763	257/E21.1		Fitzgerald; Eugene	P						
34		US 6713326	2004033	14	Process for producing se	438/149	257/E21.1		Cheng; Zhi-Yuan et	P						
35		US 6703688	2004030	29	Relaxed silicon germaniu	257/616	257/190;		Fitzgerald; Eugene	P						
36		US 6703144	2004030	16	Heterointegration of mate	428/641	117/953;		Fitzgerald; Eugene	P						
37		US 6689211	2004021	28	Etch stop layer system	117/94	117/915;		Wu; Kenneth C. et	P						
38		US 6680495	2004012	17	Silicon wafer with embed	257/183	257/184;		Fitzgerald; Eugene	P						

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U	I	Document	Issue Date	Page	Title	Current O	Current X	Retrieval	Inventor	S	C	P	2	3	4
39	r	US 6677655	20040111	16	Silicon wafer with embed	257/432	257/186;		Fitzgerald; Eugene	<input checked="" type="checkbox"/>					
40	r	US 6649480	20031111	24	Method of fabricating C	438/285	257/E21.6		Fitzgerald, Eugene	<input checked="" type="checkbox"/>					
41	r	US 6642536	2003110	11	Hybrid silicon on insulat	257/19	257/20;		Xiang; Qi et al.	<input checked="" type="checkbox"/>					
42	r	US 6633066	2003101	31	CMOS integrated circuit	257/347	257/348;		Bae; Geum-jong et	<input checked="" type="checkbox"/>					
43	r	US 6607948	2003081	18	Method of manufacturing	438/151	438/938		Sugiyama; Naoharu	<input checked="" type="checkbox"/>					
44	r	US 6603156	2003080	6	Strained silicon on insula	257/190	257/347;		Rim; Kern	<input checked="" type="checkbox"/>					
45	r	US 6602613	2003080	14	Heterointegration of mate	428/641	117/953;		Fitzgerald; Eugene	<input checked="" type="checkbox"/>					
46	r	US 6597016	2003072	26	Semiconductor device an	257/77	257/289;		Yuki; Koichiro et al	<input checked="" type="checkbox"/>					
47	r	US 6593641	2003071	26	Relaxed silicon germaniu	257/616	257/18;		Fitzgerald; Eugene	<input checked="" type="checkbox"/>					
48	r	US 6573126	2003060	13	Process for producing se	438/149	257/E21.5		Cheng; Zhi-Yuan et	<input checked="" type="checkbox"/>					
49	r	US 6555839	2003042	20	Buried channel strained s	257/18	257/19;		Fitzgerald; Eugene	<input checked="" type="checkbox"/>					
50	r	US 6521041	2003021	20	Etch stop layer system	117/94	117/915;		Wu; Kenneth C. et	<input checked="" type="checkbox"/>					
51	r	US 6495402	2002121	8	Semiconductor-on-insula	438/149	257/E21.4		Yu; Bin et al.	<input checked="" type="checkbox"/>					
52	r	US 6455871	2002092	10	SiGe MODFET with a m	257/12	257/189;		Shim; Kyu Hwan et	<input checked="" type="checkbox"/>					
53	r	US 6410371	2002062	7	Method of fabrication of	438/151	257/E21.4		Yu; Bin et al.	<input checked="" type="checkbox"/>					
54	r	US 6380590	2002043	7	SOI chip having multiple	257/350	257/289;		Yu; Bin	<input checked="" type="checkbox"/>					
55	r	US 6350993	2002022	22	High speed composite p-	257/19	257/18;		Chu; Jack Oon et al	<input checked="" type="checkbox"/>					
56	r	US 6326667	2001120	13	Semiconductor devices a	257/347	257/18;		Sugiyama; Naoharu	<input checked="" type="checkbox"/>					
57	r	US 6310367	2001103	32	IMOS transistor having a	257/190	257/19		Yaoishita; Atsushi et	<input checked="" type="checkbox"/>					

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